SONY

CXP818P48A

CMOS 8-bit Single Chip Microcomputer

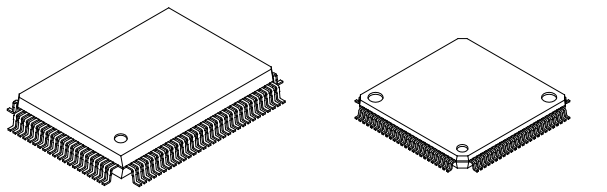
Description

The CXP818P48A is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, 32kHz timer/event counter, remote control receiving circuit, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also CXP818P48A provides sleep/stop function which enables to lower power consumption and ultra low speed instruction mode in 32kHz operation.

This IC is the PROM-incorporated version of the CXP81848A with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

100 pin QFP (PIastic) 100 pin LQFP (PIastic)



Structure

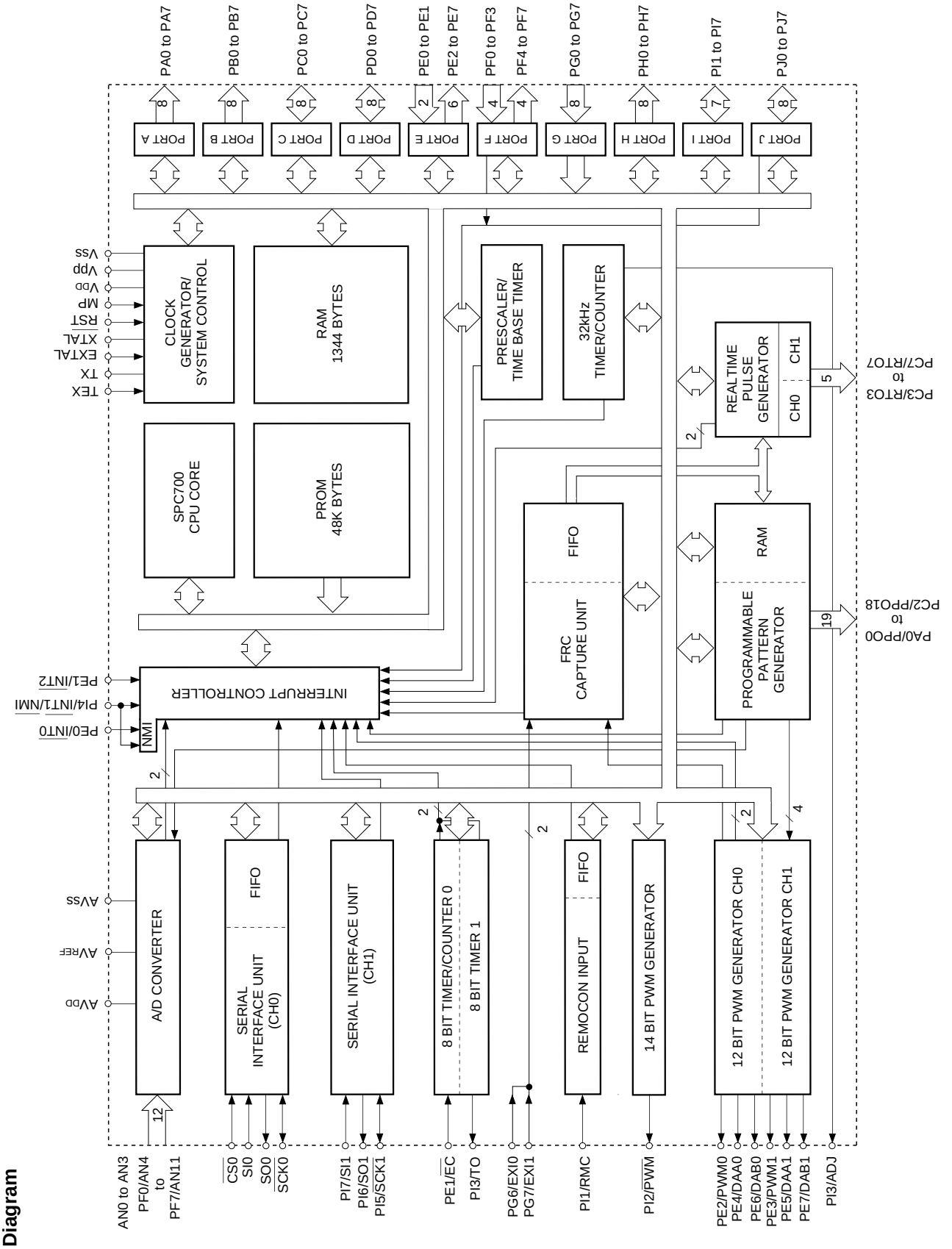
Silicon gate CMOS IC

Features

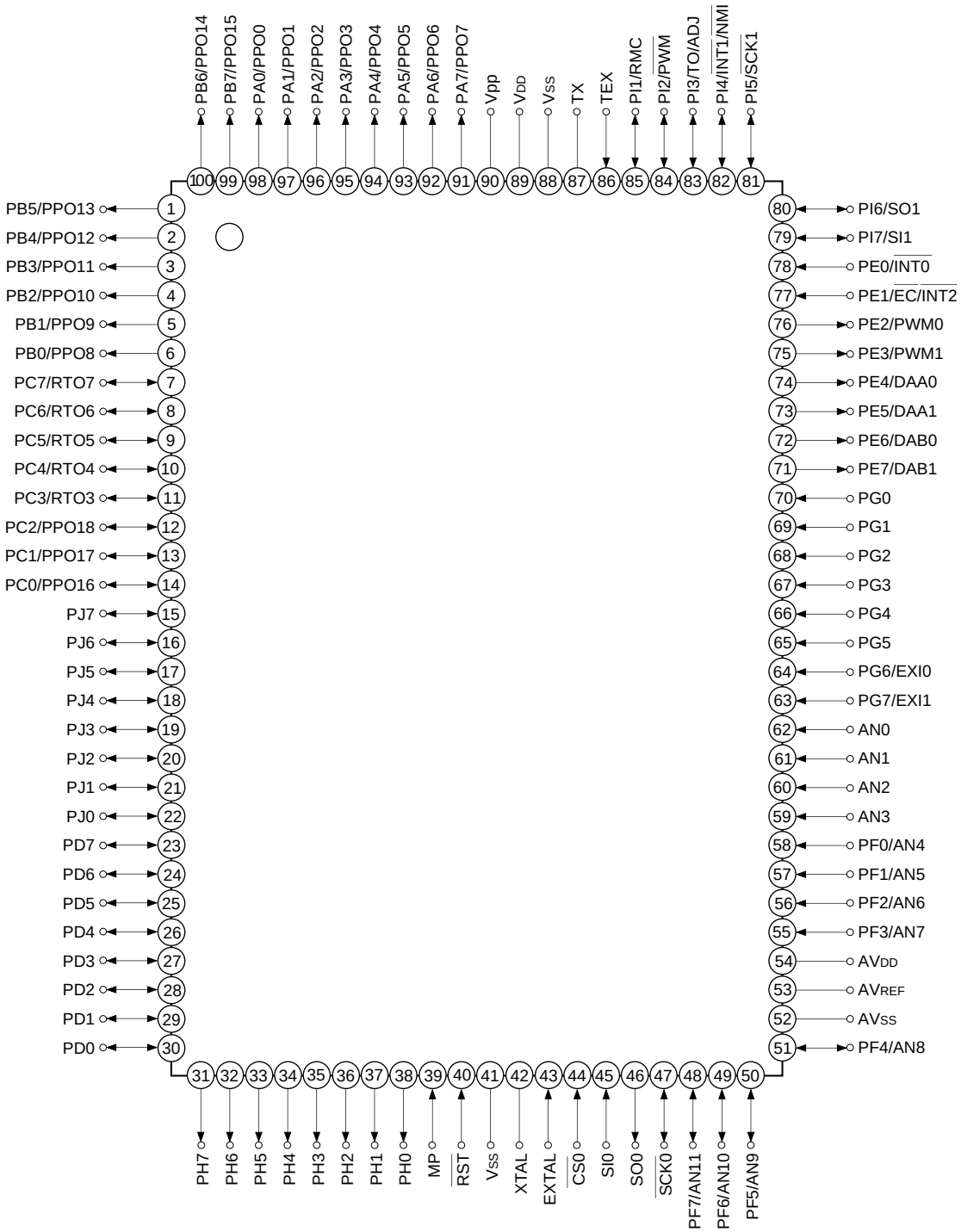
- A wide instruction set (213 instructions) which cover various types of data
  — 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle — During operation 333ns/12MHz (Supply voltage 3.0 to 5.5V)
  During operation 250ns/16MHz (Supply voltage 4.5 to 5.5V)
  During operation 122µs/32kHz
- Incorporated PROM capacity — 48Kbytes
- Incorporated RAM capacity — 1344bytes
- Peripheral functions
  - — A/D converter — 8-bit, 12-channel, successive approximation system (Conversion time 20.0µs/16MHz)
  - — Serial interface — Incorporated 8-bit and 8-stage FIFO, 1-channel (1 to 8 bytes auto transfer)
    8-bit serial I/O, 1-channel
  - — Timer — 8-bit timer, 8-bit timer/counter, 19-bit time base timer
    32kHz timer/counter
  - — High precision timing pattern generator — PPG 19 pins 32-stage programmable
    RTG 5-pins 2-channel
  - — PWM/DA gate output — 12-bit, 2-channel (Repetitive frequency 62kHz/16MHz)
  - — FRC capture unit — Incorporated 26-bit and 8-stage FIFO
  - — PWM output — 14-bit, 1-channel
  - — Remote control receiving circuit — 8-bit pulse measuring counter, 6-stage FIFO
- Interruption — 20 factors, 15 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 100-pin plastic QFP/LQFP

E94Z13-ST

Block Diagram

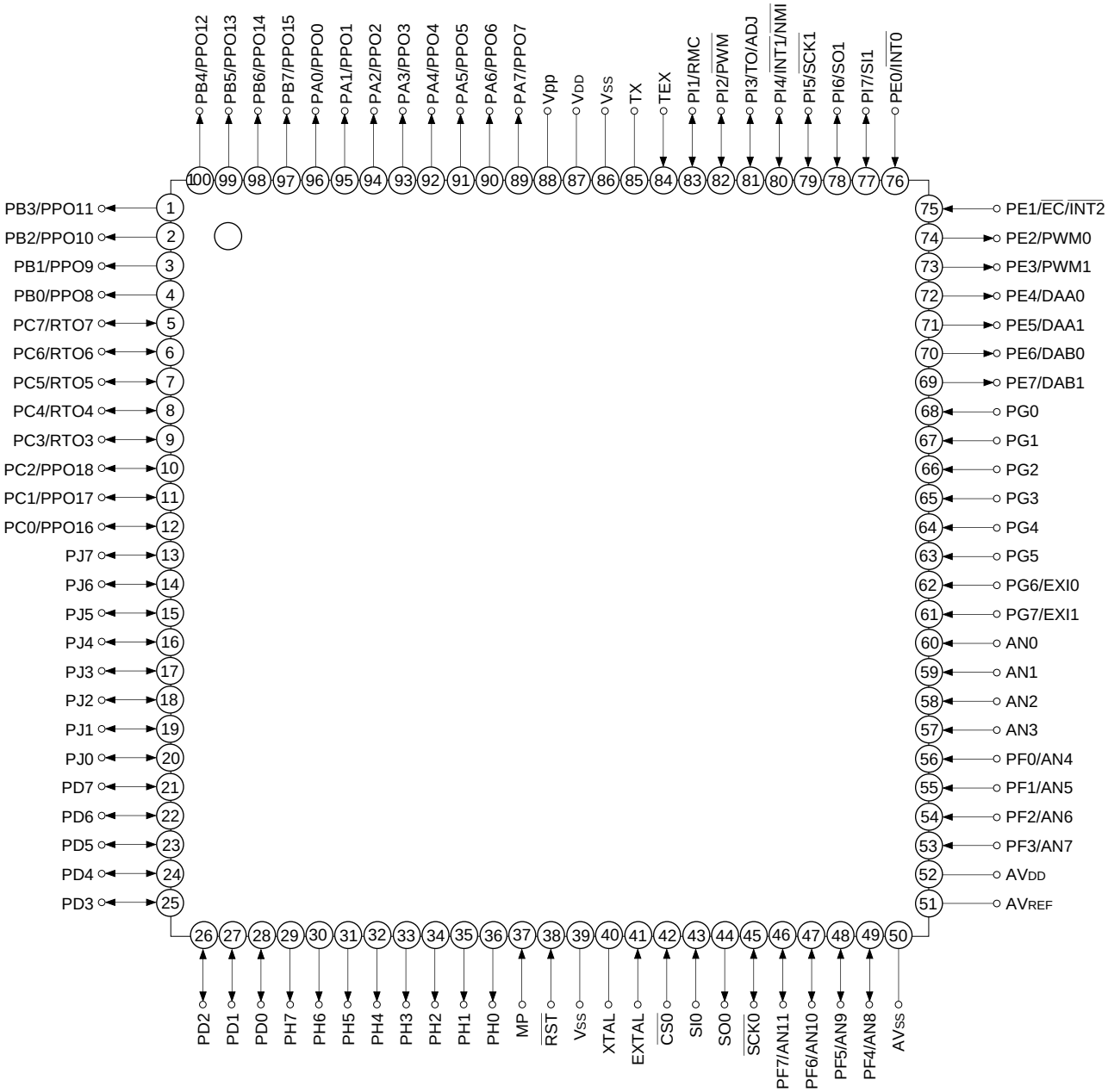


Pin Configuration 1 (Top View) 100 pin QFP package



Note) 1. Vpp (Pin 90) is always connected to V_{DD}.
2. Vss (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100 pin LQFP package



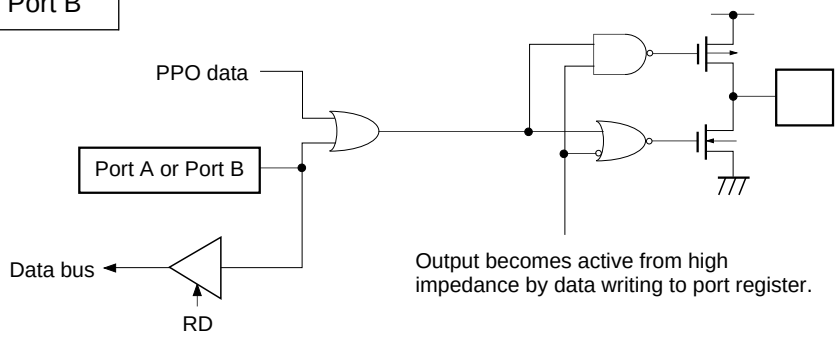
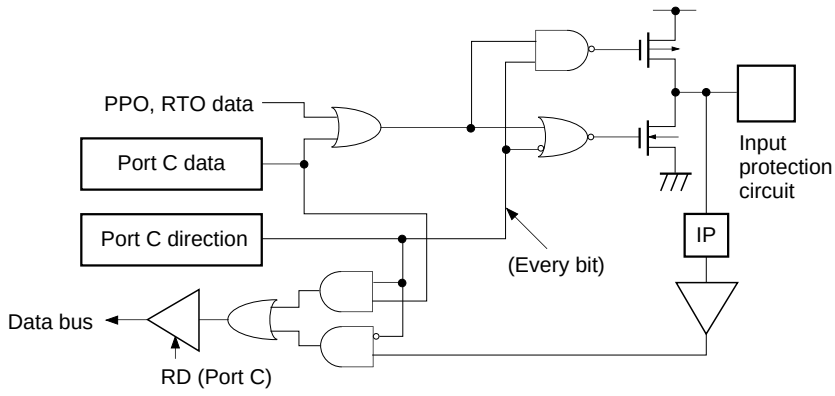
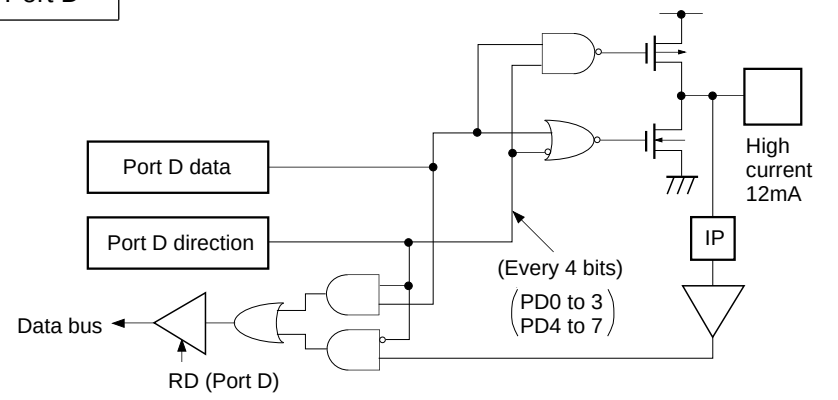
Note) 1. Vpp (Pin 88) is always connected to V_{DD}.
2. Vss (Pins 39 and 86) are both connected to GND.

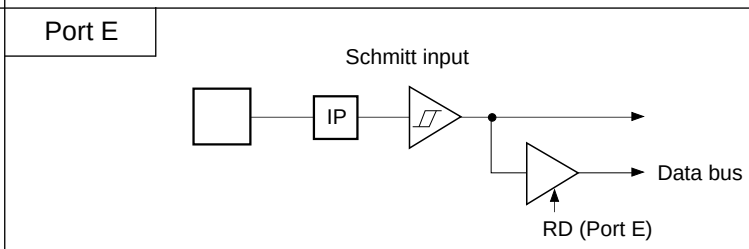
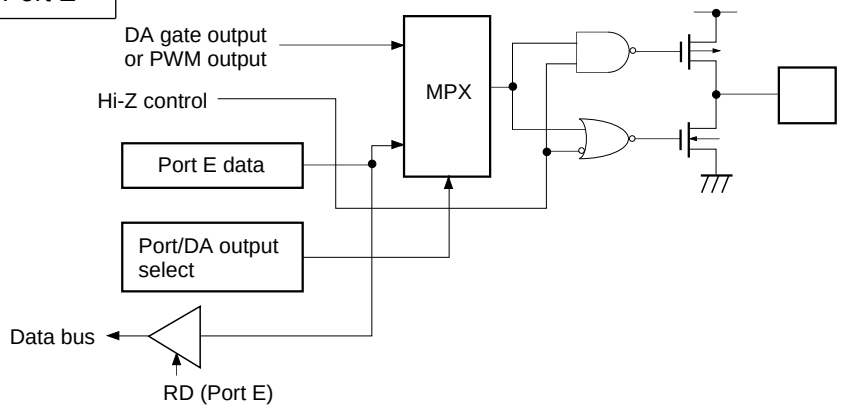
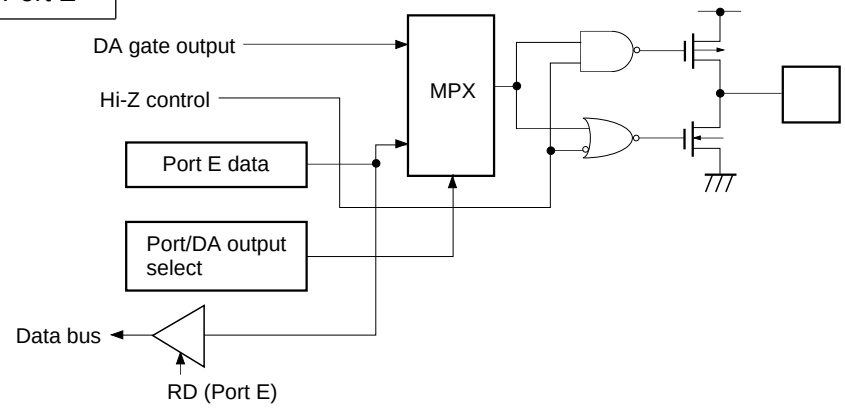
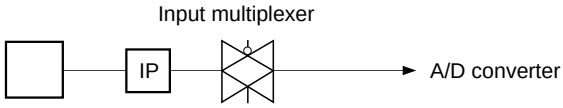
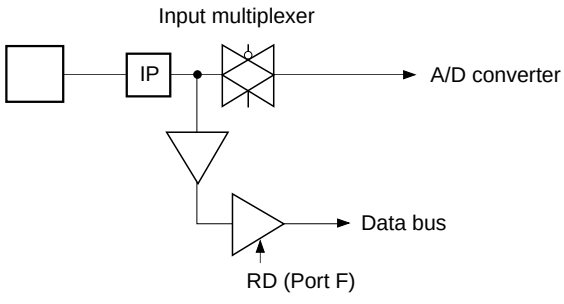
Pin Description

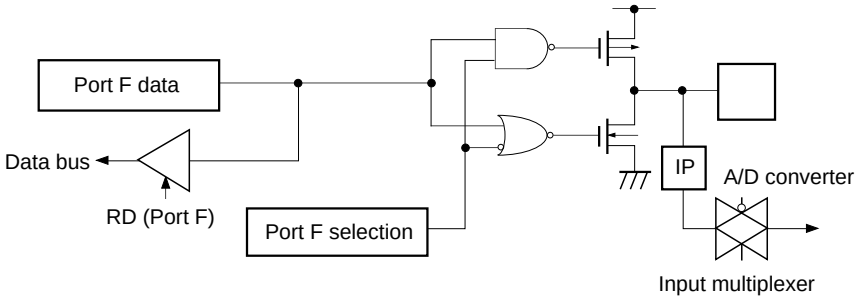
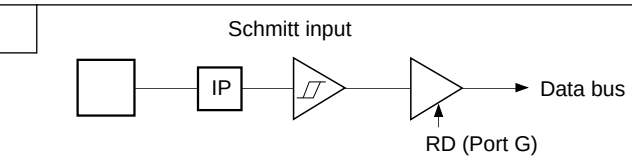
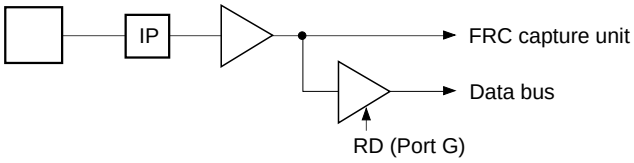
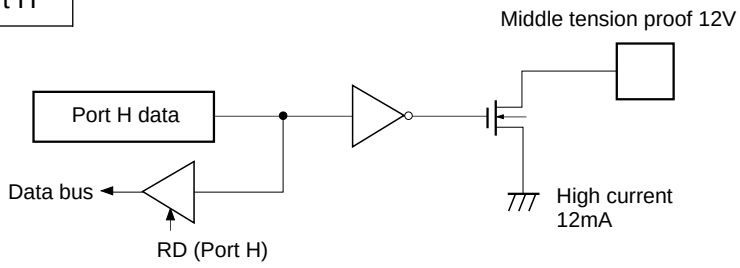
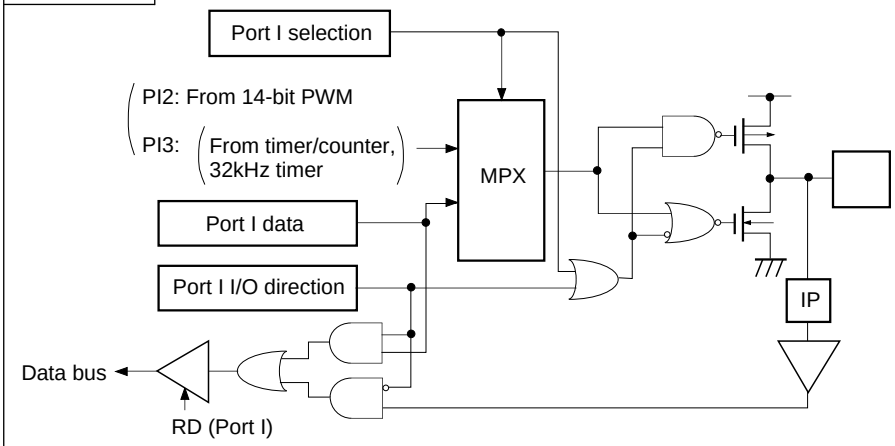
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td>PA0/PPO0
to
PA7/PPO7</td><td>Output/
Real time
Output</td><td>(Port A)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td><td colspan="2" rowspan="3">Programmable pattern generator (PPG) output.
Functions as high precision real time pulse output port.
(19 pins)</td></tr>
<tr><td>PB0/PPO8
to
PB7/PPO15</td><td>Output/
Real time
Output</td><td>(Port B)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC0/PPO16
to
PC2/PPO18</td><td>I/O/
Real time
Output</td><td rowspan="2">(Port C)
8-bit I/O port, enables to specify I/O by bit unit.
Data is gated with PPO or RTO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC3/RTO3
to
PC7/RTO7</td><td>I/O/
Real time
Output</td><td colspan="2">Real time pulse generator (RTG) output.
Functions as high precision real time pulse output port. (5 pins)</td></tr>
<tr><td>PD0 to PD7</td><td>I/O</td><td colspan="3">(Port D)
8-bit I/O port. Enable to specify I/O by 4-bit unit.
Enables to drive 12mA sink current.
(8 pins)</td></tr>
<tr><td>PE0/$\overline{INT0}$</td><td>Input/input</td><td rowspan="8">(Port E)
8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins.
(8 pins)</td><td colspan="2">Input pin to request external interruption.
Active when falling edge.</td></tr>
<tr><td>PE1/$\overline{EC}$/$\overline{INT2}$</td><td>Input/input/input</td><td>External event input pin for timer/counter.</td><td>Input pin to request external interruption.
Active when falling edge.</td></tr>
<tr><td>PE2/PWM0</td><td>Output/output</td><td colspan="2" rowspan="2">PWM output pins.
(2 pins)</td></tr>
<tr><td>PE3/PWM1</td><td>Output/output</td></tr>
<tr><td>PE4/DAA0</td><td>Output/output</td><td colspan="2" rowspan="4">DA gate pulse output pins.
(4 pins)</td></tr>
<tr><td>PE5/DAA1</td><td>Output/output</td></tr>
<tr><td>PE6/DAB0</td><td>Output/output</td></tr>
<tr><td>PE7/DAB1</td><td>Output/output</td></tr>
<tr><td>AN0 to AN3</td><td>Input</td><td colspan="3">Analog input pins to A/D converter. (12 pins)</td></tr>
<tr><td>PF0/AN4
to
PF3/AN7</td><td>Input/input</td><td colspan="3" rowspan="2">(Port F)
Lower 4 bits are input port and upper 4 bits are output port.
Lower 4 bits also serve as standby release input pin.
(8 pins)</td></tr>
<tr><td>PF4/AN8
to
PF7/AN11</td><td>Output/input</td></tr>
<tr><td>$\overline{SCK0}$</td><td>I/O</td><td colspan="3">Serial clock (CH0) I/O pin.</td></tr>
<tr><td>SO0</td><td>Ouput</td><td colspan="3">Serial data (CH0) output pin.</td></tr>
<tr><td>SI0</td><td>Input</td><td colspan="3">Serial data (CH0) input pin.</td></tr>
<tr><td>$\overline{CS0}$</td><td>Input</td><td colspan="3">Serial chip select (CH0) input pin.</td></tr>
</table>

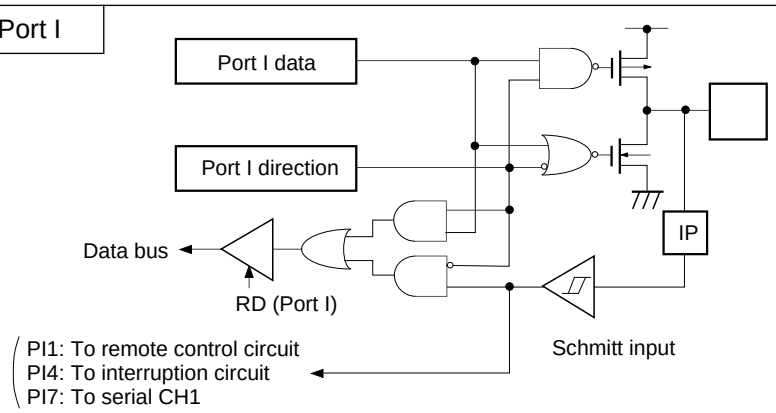
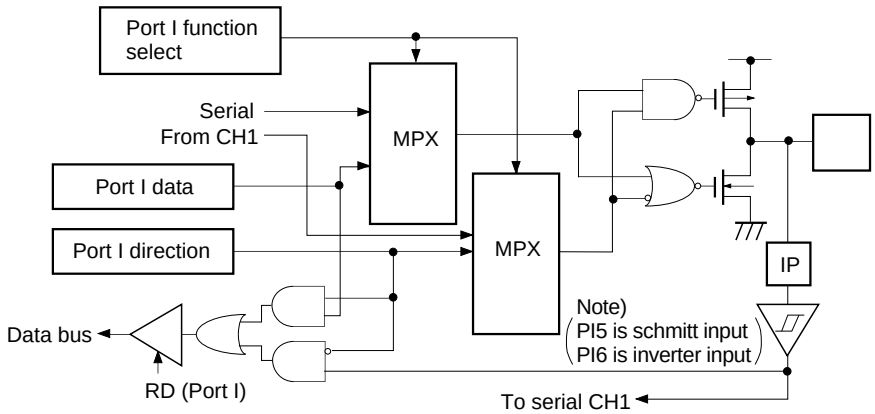
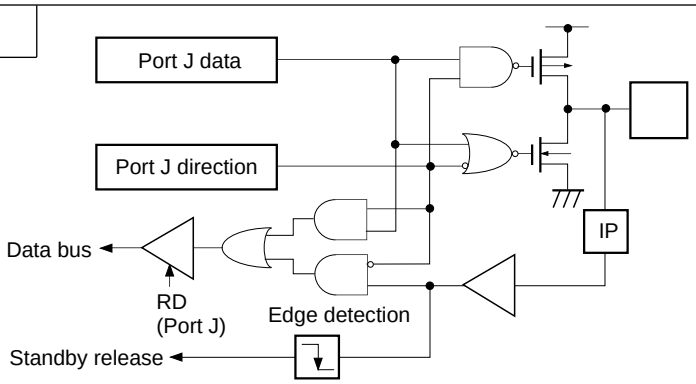
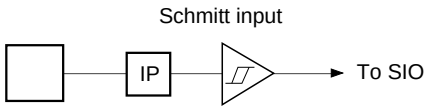
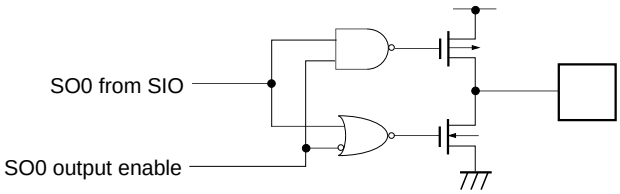
Symbol	I/O	Description	
PG0 to PG5	Input	(Port G) 8-bit input port. (8 pins)	
PG6/EXI0	Input/input		External input pin to FRC capture unit.
PG7/EXI1	Input/input		
PH0 to PH7	Output	(Port H) N-ch open drain output of middle tension proof (12V) and high current (12mA). (8 pins)	
PI1/RMC	I/O/input	(Port I) 7-bit I/O port. I/O port can be specified by the bit unit. (7 pins)	Remote control receiving circuit input pin.
PI2/$\overline{\text{PWM}}$	I/O/output		14-bit PWM output pin.
PI3/TO/ADJ	I/O/output/output		Timer/counter, 32kHz oscillation adjustment output pin.
PI4/$\overline{\text{INT1}}$/$\overline{\text{NMI}}$	I/O/input/input		Input pin to request external interruption and non maskable interruption. Active when falling edge.
PI5/$\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/output		Serial data (CH1) output pin.
PI7/SI1	I/O/input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by the bit unit. I/O can be specified by the bit unit.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
$\overline{\text{RST}}$	Input	System reset pin of active "Low" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV_{DD}		Positive power supply pin of A/D converter.	
AV_{REF}	Input	Reference voltage input pin of A/D converter.	
AVss		GND pin of A/D converter.	
V_{DD}		Positive power supply pin.	
Vpp		V_{CC} supply for writing of built-in PROM. Under normal operating conditions, connect to V_{DD}.	
Vss		GND pin. Connect both Vss pins to GND.	

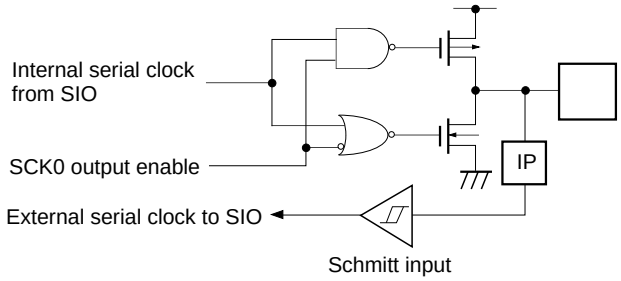
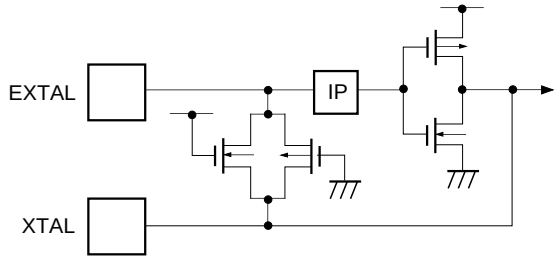
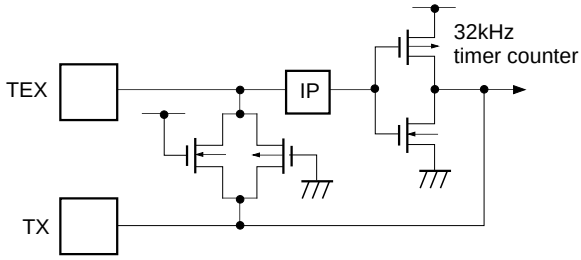
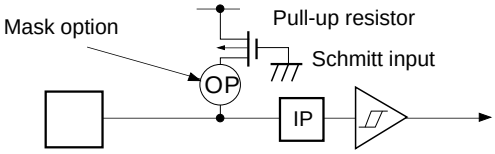
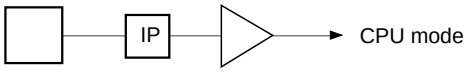
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15 16 pins	Port A Port B 	Hi-Z
PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7 8 pins	Port C 	Hi-Z
PD0 to PD7 8 pins	Port D 	Hi-Z

Pin	Circuit format	When reset
PE0/$\overline{INT0}$ PE1/$\overline{EC}$/$\overline{INT2}$ 2 pins	Port E 	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	H level
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z

Pin	Circuit format	When reset
PF4/AN8 to PF7/AN11 4 pins	Port F 	Hi-Z
PG0 to PG5 6 pins	Port G  Note) For PG4 and PG5 input format, there are CMOS schmitt input and TTL schmitt input with product.	Hi-Z
PG6/EXI0 PG7/EXI1 2 pins	Port G 	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z
PI2/$\overline{\text{PWM}}$ PI3/TO/ADJ 2 pins	Port I 	Hi-Z

PIn	Circuit format	When reset
PI1/RMC PI4/$\overline{\text{INT1}}$/$\overline{\text{NMI}}$ PI7/SI1 3 pins	Port I 	Hi-Z
PI5/$\overline{\text{SCK1}}$ PI6/SO1 2 pins	Port I 	Hi-Z
PJ0 to PJ7 8 pins	Port J 	Hi-Z
$\overline{\text{CS0}}$ SI0 2 pins		Hi-Z
SO0 1 pin		Hi-Z

PIn	Circuit format	When reset
$\overline{SCK0}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL becomes "H" level.	Oscillation
TEX TX 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level.	Oscillation
$\overline{RST}$ 1 pin		L level
MP 1 pin		Hi-Z

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13	V	Incorporated PROM
	AV_{DD}	AVss to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
Medium withstand output voltage	V_{OUTP}	–0.3 to +15.0	V	PH pin
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than high current output pins: per pin
	I_{OLC}	20	mA	High current port pin*3: per pin
Low level total output current	$\sum I_{OL}$	130	mA	Total of output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package type
		380		LQFP package type

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*3 The high current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks	
Supply voltage	V_{DD}	4.5	5.5	V	fc = less than 16MHz	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.0	5.5	V	fc = less than 12MHz	
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation	
		2.7	5.5	V	Guaranteed operation range by TEX clock	
		2.5	5.5	V	Guaranteed data hold operation range during STOP	
	Vpp	Vpp = V_{DD}		V	*9	
Analog power supply	AV_{DD}	3.0	5.5	V	*1	
HIgh level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS schmitt input*3	
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input*4, *7	
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*5, *7 TEX pin*6, *7	
		V_{DD} – 0.2	V_{DD} + 0.2	V	EXTAL pin*5, *8 TEX pin*6, *8	
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2, *7	
		0	0.2V_{DD}	V	*2, *8	
	V_{ILS}	0	0.2V_{DD}	V	CMOS schmitt input*3	
	V_{ILTS}	0	0.8	V	TTL schmitt input*4, *7	
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*5, *7 TEX pin*6, *7	
		–0.3	0.2	V	EXTAL pin*5, *8 TEX pin*6, *8	
Operating temperature	Topr	–20	+75	°C		

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (Each pin of PC, PD, PE0, PE1, PF0 to PF3, PG, PI and PJ), MP pin.

*3 Each pin of $\overline{CS0}$, SI0, $\overline{SCK0}$, $\overline{RST}$, PE0/$\overline{INT0}$, PE1/$\overline{EC}$/$\overline{INT2}$, PG (When PG4 and PG5, are CMOS schmitt input product), PI1/RMC, PI4/$\overline{INT1}$/$\overline{NMI}$, PI5/$\overline{SCK1}$ and PI7/SI1.

*4 Each pin of PG4 and PG5 (When they are TTL schmitt input product).

*5 It specifies only when the external clock is input.

*6 It specifies only when the event count clock is input.

*7 This case applies to the range of 4.5 to 5.5V supply voltage (V_{DD}).

*8 This case applies to the range of 3.0 to 3.6V supply voltage (V_{DD}).

*9 Vpp and V_{DD} should be set to a same voltage.

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta = –10 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$		–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$, $\overline{RST}$	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-CH Tr OFF in state)	I_{LOH}	PH	V_{DD} = 5.5V, V_{OH} = 12V			50	µA
Supply current*1	I_{DD1}	V_{DD}	16MHz crystal oscillation (C_1 = C_2 = 15pF), V_{DD} = 5V ± 0.5V*2		24	45	mA
	I_{DDS1}		SLEEP mode, V_{DD} = 5V ± 0.5V		1.5	8	mA
	I_{DD2}		32kHz crystal oscillation (C_1 = C_2 = 47pF), V_{DD} = 3V ± 0.3V		430	1000	µA
	I_{DDS2}		SLEEP mode, V_{DD} = 3V ± 0.3V		9	30	µA
	I_{DDS3}		STOP mode (EXTAL pin and TEX pin oscillation stop), V_{DD} = 5V ± 0.5V			10	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss	Clock 1MHz, 0V other than the measured pins		10	20	pF

*1 When entire output pins are open.

*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE$_H$) to "00" and operating in high speed mode (1/2 dividing clock).

DC Characteristics (V_{DD} = 3.0 to 3.6V) (Ta = –10 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	V_{DD} = 3.0V, I_{OH} = –0.15mA	2.7			V
			V_{DD} = 3.0V, I_{OH} = 0.5mA	2.3			V
Low level output voltage	V_{OL}		V_{DD} = 3.0V, I_{OL} = 1.2mA			0.3	V
			V_{DD} = 3.0V, I_{OL} = 1.6mA			0.5	V
		PD, PH	V_{DD} = 3.0V, I_{OL} = 5mA			1.0	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.6V, V_{IH} = 3.6V	0.3		20	µA
	I_{ILE}		V_{DD} = 3.6V, V_{IL} = 0.3V	–0.3		–20	µA
	I_{IHT}	TEX	V_{DD} = 3.6V, V_{IH} = 3.6V	0.1		10	µA
	I_{ILT}		V_{DD} = 3.6V, V_{IL} = 0.3V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$		–0.9		–200	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$, $\overline{RST}$	V_{DD} = 3.6V, V_I = 0, 3.6V			±10	µA
Open drain output leakage current	I_{LOH}	PH	V_{DD} = 3.6V, V_{OH} = 12V			50	µA
Supply current*1	I_{DD1}	V_{DD}	12MHz crystal oscillation (C_1 = C_2 = 15pF) V_{DD} = 3.3V ± 0.3V*2		12	25	mA
	I_{DDS1}		SLEEP mode V_{DD} = 3.3V ± 0.3V		0.7	2.5	mA
	I_{DDS3}		STOP mode (EXTAL pin and TEX pin oscillation stop) V_{DD} = 3.3V ± 0.3V			30	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 When entire output pins are open.

*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: $00FE_H$) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

($Ta = -10$ to $+75°C$, $V_{DD} = 3.0$ to $5.5V$, $Vss = 0V$)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2 V_{DD} = 4.5 to 5.5V	1	16	MHz
			Fig. 1, Fig. 2	1	12	
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, V_{DD} = 4.5 to 5.5V	28		ns
			Fig. 1, Fig. 2 (External clock drive)	37.5		
System clock input rise and fall times	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	$tsys \times 4$*		ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3		20	ns
System clock frequency	f_C	TEX TX	Fig. 2 V_{DD} = 2.7 to 5.5V (32kHz clock applied condition)	32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10		µs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3		20	ms

* tsys indicates three values according to the contents of the clock control register (address; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

Fig. 1. Clock timing

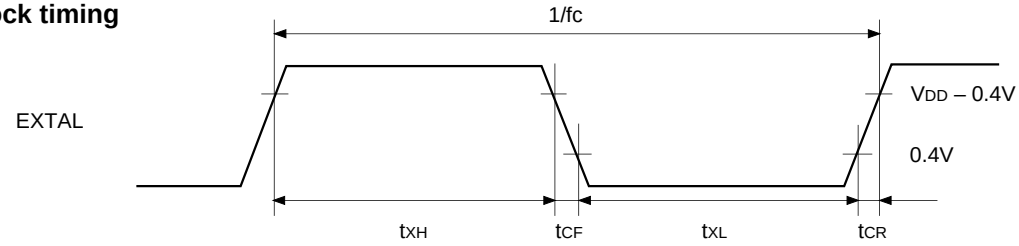


Fig. 2. Clock applied condition

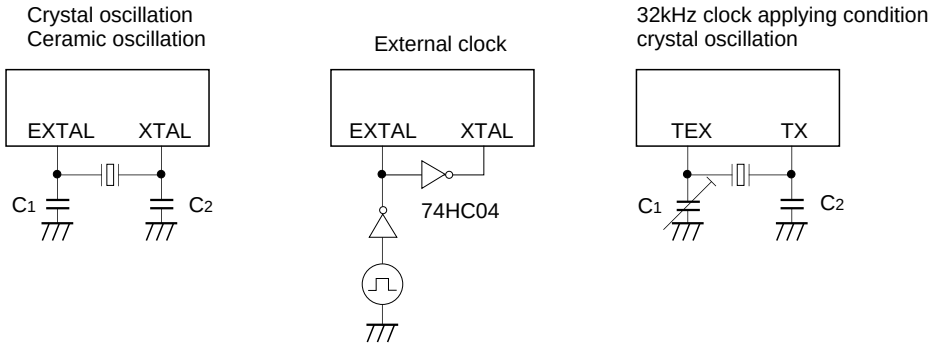
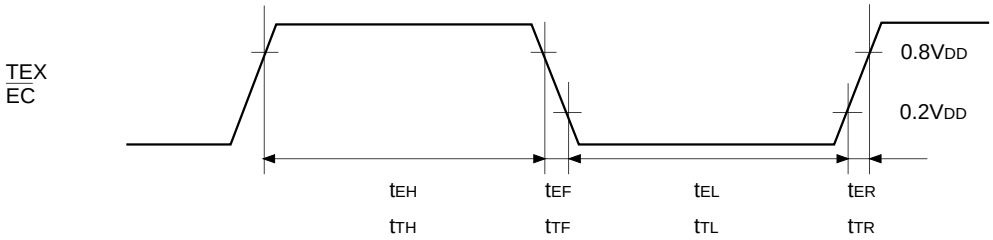


Fig. 3. Event count clock timing



(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}\downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0}\uparrow \rightarrow \overline{SCK0}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0}\downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}\uparrow \rightarrow$ SO0 floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 input setup time (against $\overline{SCK0}\uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0}\uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0}\downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF + 1TTL.

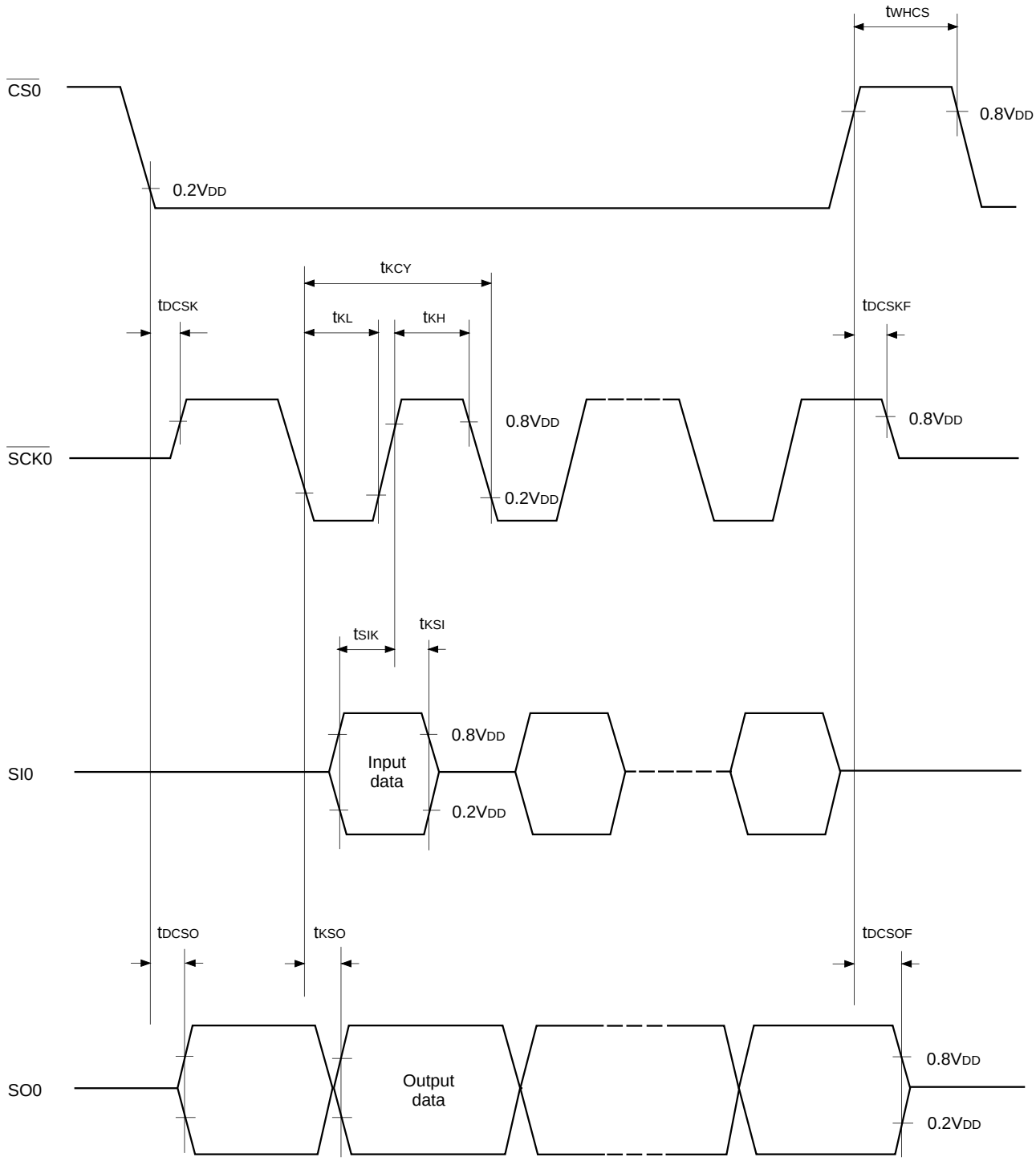
Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}\downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 250	ns
$\overline{CS0}\uparrow \rightarrow \overline{SCK0}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0}\downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 250	ns
$\overline{CS0}\uparrow \rightarrow$ SO0 floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI0 input setup time (against $\overline{SCK0}\uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0}\uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0}\downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 250	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF.

Fig. 4. Serial transfer CH0 timing



Serial transfer (CH1) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	8000/fc – 50		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

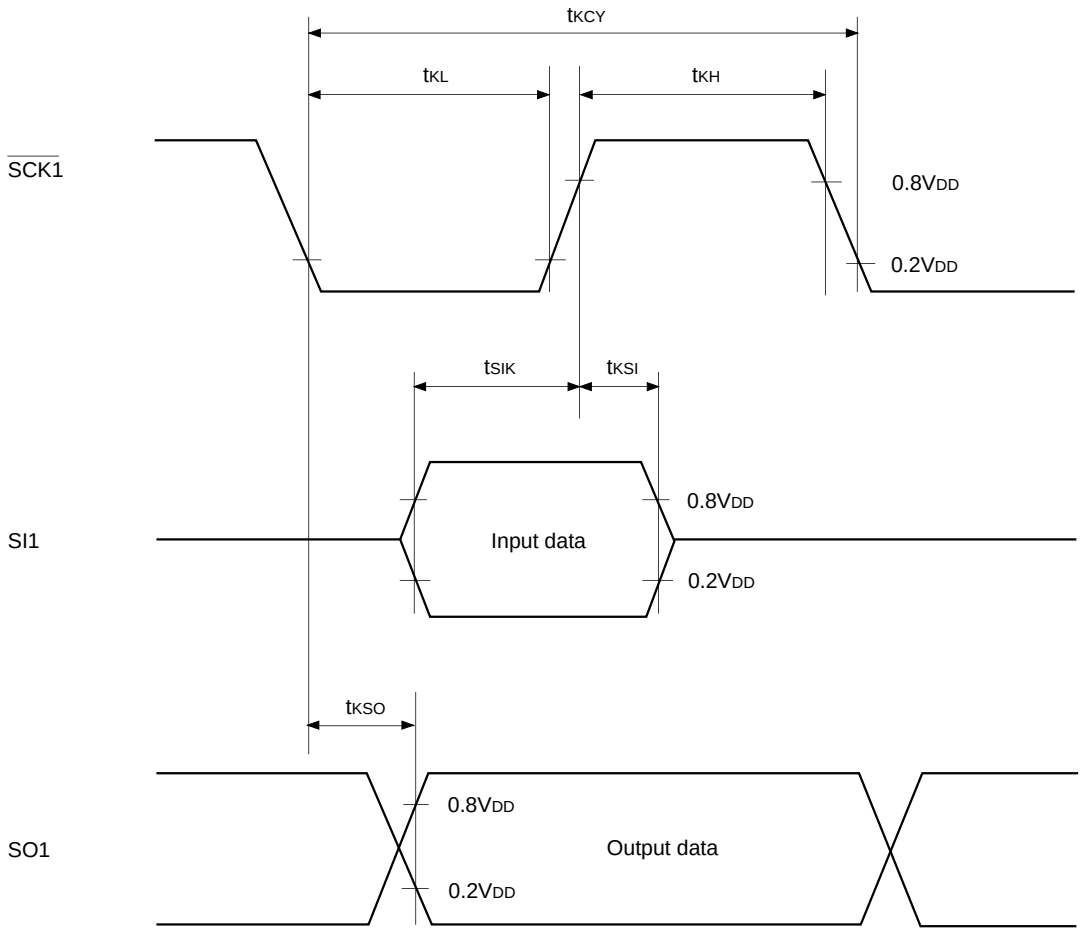
Note) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.

Serial transfer (CH1) (Ta = –10 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	8000/fc – 100		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		250	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing



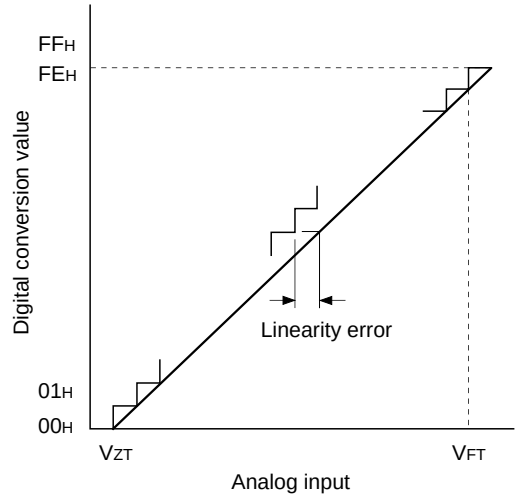
(3) A/D converter characteristics (Ta = –10 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}*			µs
Sampling time	t_{SAMP}			12/f_{ADC}*			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 4.5 to 5.5V	AV_{DD} – 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	µA

(Ta = –10 to +75°C, V_{DD} = AV_{DD} = 3.0 to 3.6V, AV_{REF} = 2.7 to AV_{DD}, Vss = AV_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}*			µs
Sampling time	t_{SAMP}			12/f_{ADC}*			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = 3.0 to 3.6V	AV_{DD} – 0.3		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.4	0.7	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	µA

Fig. 6. Definitions of A/D converter terms



* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).
When PS2 is selected, f_{ADC} = fc/2
When PS1 is selected, f_{ADC} = fc

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$ PJ0 to PJ7		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

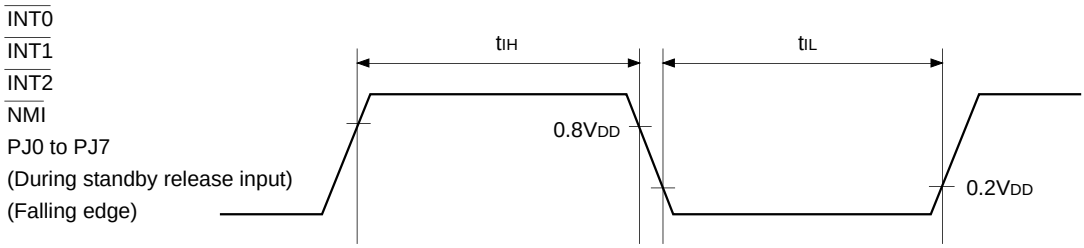
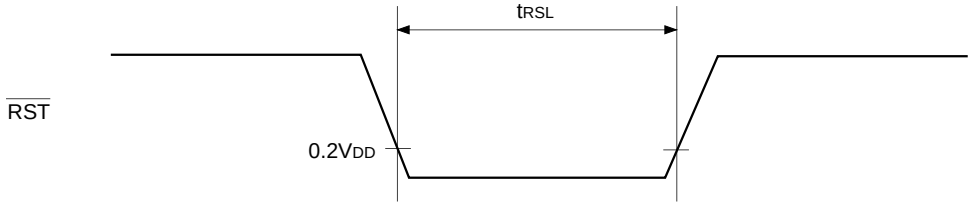


Fig. 8. Reset input timing

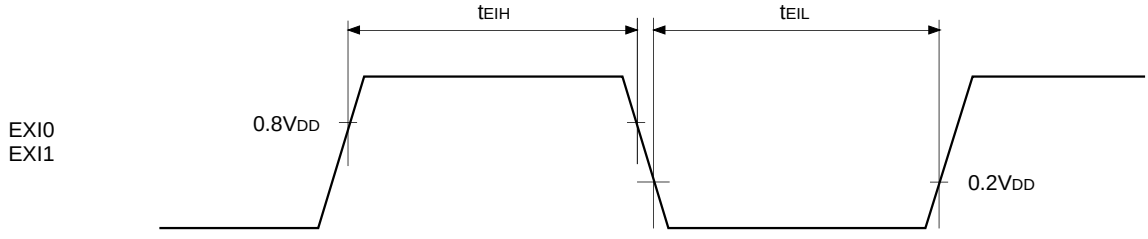


(5) Others (Ta = –10 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
EXI input high and low level widths	t_{EIH}	EXI0 EXI1	tsys = 2000/fc	$t_{FRC} \times 8 + 200 + t_{sys}$		ns

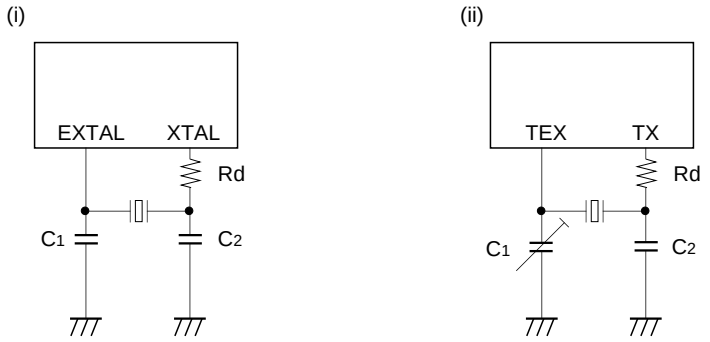
Note) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")
t_{FRC} [ns] = 1000/fc

Fig. 9. Other timings



Supplement

Fig. 10. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	5	5		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16	12	0	(i)
		10.00	16	12		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

Those marked with an asterisk (*) signify types with built-in ground capacitance (C_1, C_2).

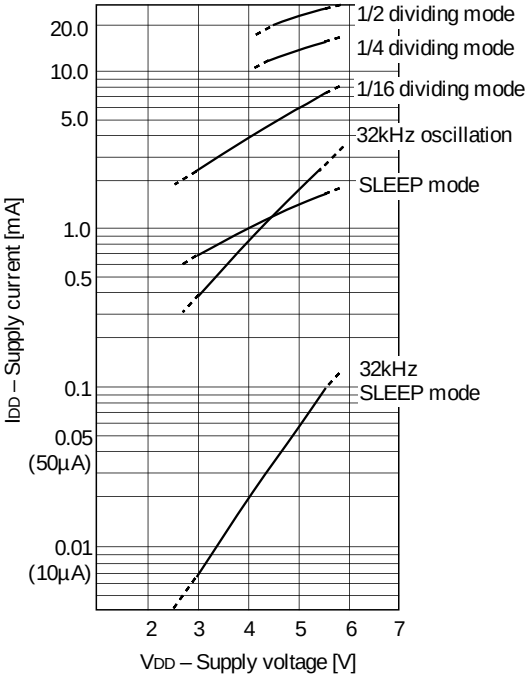
Selection Guide

Option item	Mask product						PROM product			
	CXP 81720A	CXP 81724A	CXP 81732A	CXP 81740A	CXP 81840A	CXP 81848A	CXP818P48AQ -1-□□□	CXP818P48AR -1-□□□	CXP818P48AQ -2-□□□	CXP818P48AR -2-□□□
Package	100-pin plastic QFP/LQFP						100-pin plastic QFP	100-pin plastic LQFP	100-pin plastic QFP	100-pin plastic LQFP
ROM capacitance	20K byte	24K byte	32K byte	40K byte	40K byte	48K byte	PROM 48K byte			
Reset pin pull-up resistor	Existent/Non-Existent						Existent			
Input circuit format*	CMOS schmitt/TTL schmitt						TTL schmitt	TTL schmitt	CMOS schmitt	CMOS schmitt

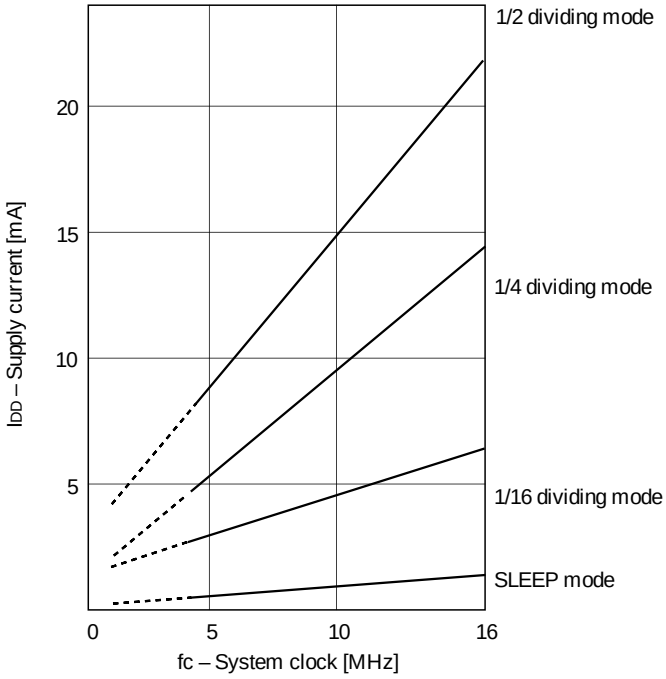
* In PG4/SYNC0 pin and PG5/SYNC1 pin.

Characteristics Curve

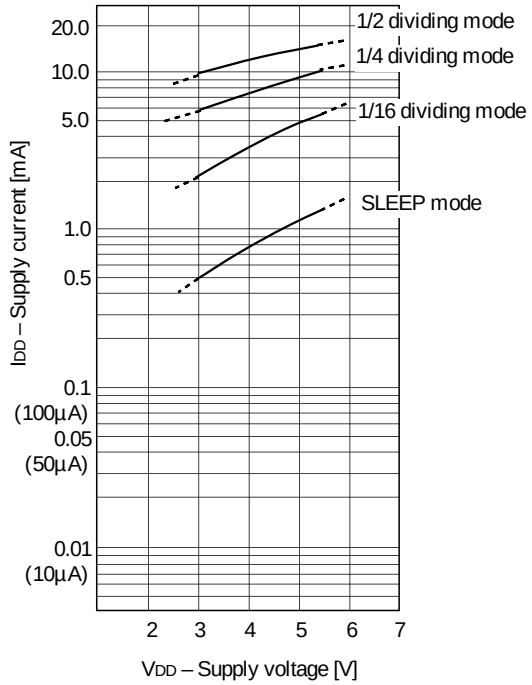
IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)



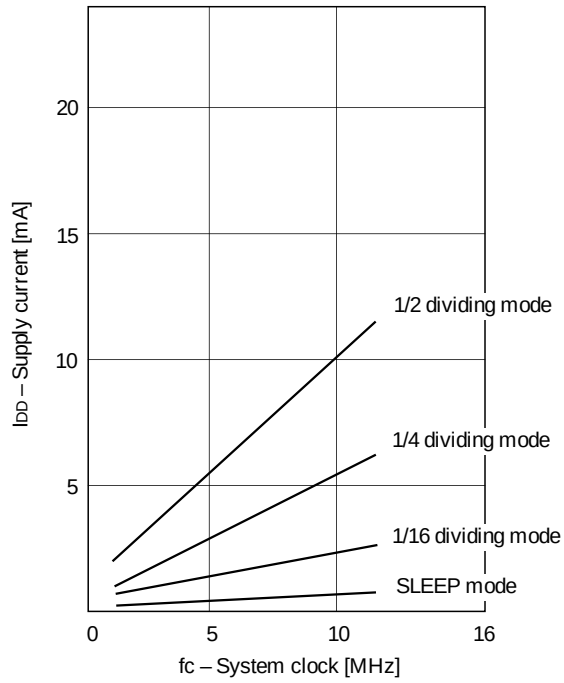
IDD vs. fc
(VDD = 5.0V, Ta = 25°C, Typical)



IDD vs. VDD
(fc = 12MHz, Ta = 25°C, Typical)

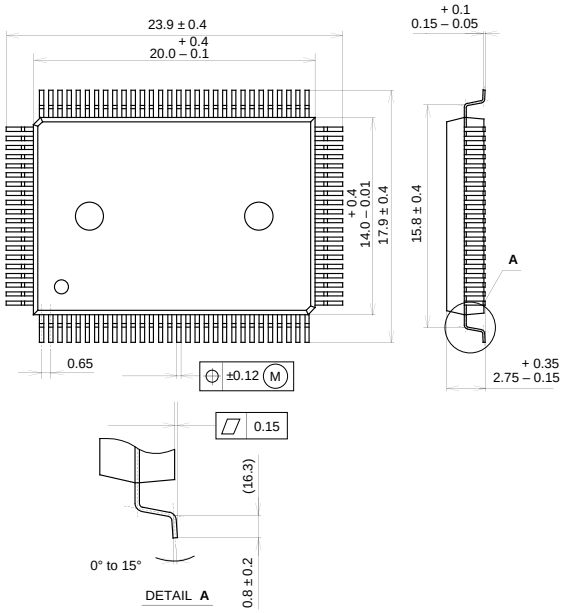


IDD vs. fc
(VDD = 3.3V, Ta = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)

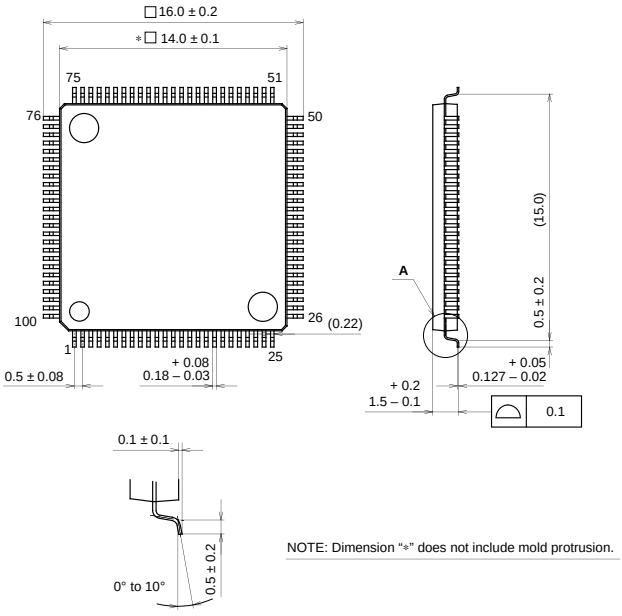


SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————